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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,178	03/31/2004	Gary Johnson	34020/US	7900

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DORSEY & WHITNEY LLP
INTELLECTUAL PROPERTY DEPARTMENT
SUITE 3400
1420 FIFTH AVENUE
SEATTLE, WA 98101

EXAMINER	
NGUYEN, HAI L	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EJC

Office Action Summary	Application No.	Applicant(s)	
	10/816,178	JOHNSON ET AL.	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,10,11,19-22,30-33,41-45 and 52-59* is/are rejected.

7)☐ Claim(s) *3-9,12-18,23-29,34-40,46-51* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *31 January 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1-2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to because they fail to label the reference numerals according to their functions, all of the reference numerals require a corresponding textual label in addition to the numeric label. For example, reference numeral 70 in Fig. 6 should be labeled as –ARBITER PHASE DETECTOR-- as described in the specification (page 11). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be

labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 25 is objected to because of the following informalities: the claim can not depend from itself. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 52 recites the limitation "The computer system" in line 1. There is insufficient antecedent basis for this limitation in the claim. Furthermore, there is no computer system in claim 41.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1 and 2 are rejected under 35 U.S.C. 102(e) as being anticipated by Suzuki (US 6,094,078).

With regard to claim 1, Larson discloses in Figs. 1-5 a phase detector (10) generating either a first control signal or a second control signal responsive to a difference in phase between a first input signal and a second input signal, the phase detector (10a, 10b) comprising a signal comparator comparing the phase of the first input signal (REFCLK) to the phase of the second input signal (DEVCLK); and a signal generator coupled to the signal comparator, the signal generator being operable to generate the first control signal (UP) responsive to the phase of the first input signal being greater than the phase of the second input signal by at least a first phase difference, and to generate the second control signal (DN) responsive to the phase of the first input signal being less than the phase of the second input signal by at least a second phase difference (see column 5, line 15 through column 6, line 45), the signal generator further being operable to generate neither the first control signal nor the second control signal responsive to either the first input signal being greater than the phase of the second input signal by less than the first phase difference or the first input signal being less than the phase of the second input signal by less than the second phase difference.

With regard to claim 2, the reference also meets the recited limitations in the claim.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 10, 11, 19-22, 30, 31, and 56-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA), Figs. 1-2 in the present application, in view of Suzuki.

With regard to claims 10 and 56, the admitted prior art, Fig. 1 in the present application, shows a delay-lock loop (10), and a method of use thereof, comprising a phase detector (14); a delay control circuit (20) coupled to the phase detector, the delay control circuit generating a delay control signal responsive to the increase and decrease control signals (16, 18) from the phase detector; and a delay circuit (24a - 24n) coupled to the delay control circuit, the delay circuit being coupled to receive the reference clock signal and to delay the reference clock signal by a variable delay to generate the feedback clock signal from the delayed reference clock signal, the delay circuit being operable to increase the magnitude of the variable delay responsive to a delay control signal generated responsive to the increase control signal and to decrease the magnitude of the variable delay responsive to a delay control signal generated responsive to the decrease control signal. Fig. 1 of the prior art meets all the claimed limitations except that the phase detector is not disclosed in detailed as the phase detector recited in the claim. Suzuki teaches in Fig. 5 a phase detector (10a, 10b) having all claimed function; note the above discussion of the phase detector with regard to claim 1. Therefore, it would have been obvious to one of ordinary skill in the art to implement the phase detector taught by Suzuki with the prior art Fig. 1 in the present application for the expected advantage of being able to arbitrarily set the range of the dead zone, which are in each case optimally matched to its application.

With regard to claims 11, 19, 20, and 57-59, the references also meet the recited limitations in these claims.

With regard to claim 21, the admitted prior art, Fig. 2 in the present application, shows a phase-lock loop (30), comprising a phase detector (14); a frequency control circuit (34) coupled to the phase detector, the frequency control circuit generating a frequency control signal ($FREQ_{CON}$) responsive to the increase and decrease control signals (16, 18) from the phase detector; and a voltage controlled oscillator (38) coupled to the frequency control circuit, the voltage controlled oscillator being operable to generate the feedback clock signal with a period that increases responsive to a frequency control signal generated responsive to the increase control signal and that decreases responsive to a frequency control signal generated responsive to the decrease control signal. Fig. 2 of the prior art meets all the claimed limitations except that the phase detector is not disclosed in detailed as the phase detector recited in the claim. Suzuki teaches in Fig. 5 a phase detector (10a, 10b) having all claimed function; note the above discussion of the phase detector with regard to claim 1. Therefore, it would have been obvious to one of ordinary skill in the art to implement the phase detector taught by Suzuki with the prior art Fig. 2 in the present application for the expected advantage of being able to arbitrarily set the range of the dead zone, which are in each case optimally matched to its application.

With regard to claims 22, 30, and 31, the references also meet the recited limitations in these claims.

10. Claims 32, 33, 41-45, and 53-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wright et al. (US 6,512,711) in view of the admitted prior art (APA), Figs. 1-2 in the present application, and Suzuki.

With regard to claim 44, Wright et al. discloses in Figs. 3&24 a computer system (2930), comprising a processor (2932); an input device (2936); an output device (2938); a data storage device (2940); a memory device (200) coupled to the processor, the memory device comprising: a row address circuit operable to receive and decode row address signals applied to external address terminals of the memory device; a column address circuit operable to receive and decode column address signals applied to the external address terminals; a memory cell array operable to store data written to or read from the array at a location determined by the decoded row address signals and the decoded column address signals; a clock generator circuit (214) operable to generate an output clock signal from a reference clock signal, the clock generator circuit. Figs. 3&24 of Wright et al. meet all the claimed limitations except that Wright et al. does not discloses the clock generator circuit in detailed as recited in the claim. It would have been obvious to one of ordinary skill in the art to implement the clock generator circuit taught by the prior arts; note the above discussion with regard to claims 10 and 56; for the expected advantage of being able to arbitrarily set the range of the dead zone, which are in each case optimally matched to its application.

Claim 32 is similarly rejected; note the above discussion with regard to claim 44.

With regard to claims 33, 41-43, 45, and 53-55, the references also meet the recited limitations in these claims.

Allowable Subject Matter

11. Claims 3-9, 12-18, 23, 24, 26-29, 34-40, and 46-51 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose or fairly suggest a phase detector circuit (80 in instant Fig. 8, as recited in claims 3, 12, 23, 34, and 20, having specific structural limitations such as a first delay circuit (84) having an output and an input coupled to receive the first input signal (CLK_REF), the first delay circuit being operable to delay the first input signal by a first delay value and couple the delayed first input signal to the output; a second delay circuit (90) having an output and an input coupled to receive the second input signal (CLK_FB), the second delay circuit being operable to delay the second input signal by a second delay value and couple the delayed second input signal to the output; a third delay circuit (88) having an output and an input coupled to receive the first input signal, the third delay circuit being operable to delay the first input signal by a third delay value and couple the delayed first input signal to the output; a fourth delay circuit (92) having an output and an input coupled to receive the second input signal, the fourth delay circuit being operable to delay the second input signal by a fourth delay value and couple the delayed second input signal to the output; a first flip-flop (upper 60) having a set input coupled to the output of the first delay circuit, a reset input coupled to the output of the second delay circuit, and a pair of complimentary first and second outputs; and a second flip-flop (lower 60) having a set input coupled to the output of the third delay circuit, a reset input coupled to the output of the fourth delay circuit, and a pair of complimentary first and

second outputs (INCR, DECR), and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Larson (US 6,392,495) is cited as of interest because it discloses a frequency detector circuits and systems.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HLN
May 26, 2005

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800